Signal and Power Integrity – A Curtain Raiser

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Abstract: *Technological advances in silicon fabrication has feature sizes of transistors as small as 17nm and expected to reach 7nm by 2017. This enables packaging more functionality on a single device. Smaller transistor geometries mean faster rise time devices. For optimized power dissipation, these devices need to operate at lower voltage. Faster devices and low operating voltages are the genesis of signal integrity and power integrity issues in digital circuits. This paper presents an overview of these aspects of digital system design.*

Key words: *Signal integrity (SI), Power integrity (PI), Reflections, Crosstalk, EMI, EMC, EYE diagram, PCB, controlled impedance.*

Introduction

Signal integrity is a critical aspect of current day high-speed digital design. It is a design challenge to system and PCB/package designers. Most of these problems are electromagnetic in nature and hence are contributing factors for EMI/EMC aspects. In this paper we will look at the generic aspects of signal and power integrity.

It is important to understand key signal integrity issues and how we can analyse and solve these issues right at the beginning of the design. The analysis task has become easier due to the availability of high performance SI and PI software tools. Key aspect of SI is to address signal timing and distortion aspects. Timing analysis is to ensure that the signal reaches the destination within the specified time window and with minimal distortion due to the interconnect effects.

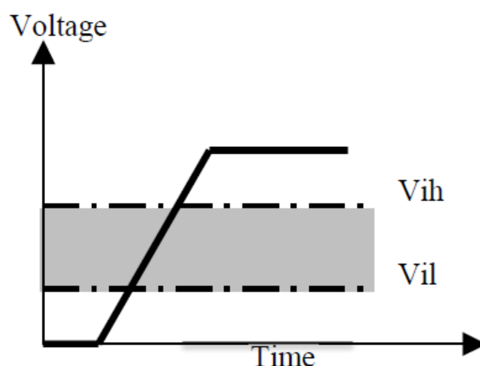

Fig 1. Logic Threshold Levels.

In a digital system, signals are validated at the receiver taking the input voltage thresholds of $\mathbf{V_{IL}}$ and $\mathbf{V_{IH}}$ as reference – Fig 1. Distortion of signal during its transmission through the interconnect may violate the threshold levels resulting in erroneous data recognition.

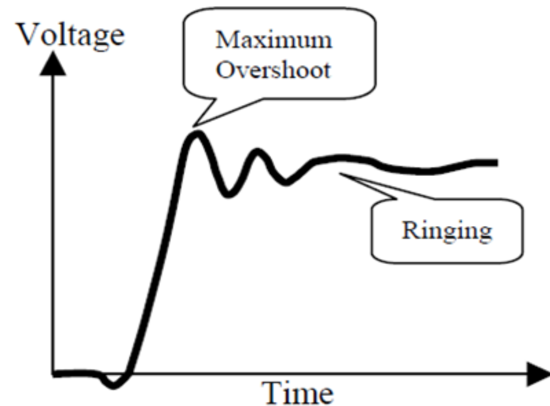

Fig 2. Signal Distortion.

Integration of more functions in a package on the silicon increases the dissipation. In order to reduce the overall package power dissipation, it has become necessary to operate at lower voltages. This reduction in operating voltage reduces the logical threshold values making signal integrity a critical aspect to be addressed in today's digital system designs. This reduction in operating voltage also has an impact on power delivery to the chip through the power planes. This introduces the aspect of power integrity to be addressed. Signal integrity affects all levels of electronics packaging, including, but not limited to, the Integrated Circuit.

Signal Integrity Basics

Signal propagation through a interconnect or package is governed by the rise time of the signal than the operating frequency. Current nano-meter silicon fabrication means faster rise/fall time devices. The band width of a interconnect is related to the rise time of the signal $\mathbf{T_r}$, and is given by the empirical formula:

$$f_{max} = \frac{0.35}{T_r}$$

In this, $\mathbf{f_{max}}$ is in MHz, and $\mathbf{T_r}$ is in nSecs. This would mean that a device with a rise time of 1nSec would require a interconnect with a bandwidth of 350MHz.

At this bandwidth, the interconnects behave as transmission lines instead of just low ohmic connections. Transmission lines are frequency dependant networks. Inherent package parasitics add R, L and C networks to the signal network. In reality the signal equivalent circuit is as shown in Fig 3.

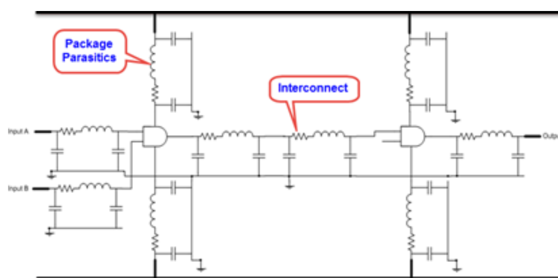

Fig 3. Equivalent Circuit of a Interconnect

Primary objective of signal integrity is to address two electrical design aspects – the timing and signal distortion. At the receiver the data is sampled at the rising edge or the falling edge of a reference clock signal. Data must arrive at the receiving gate on time and settle down to a non-ambiguous logic state when the receiving component starts to latch in. Any delay of the data or distortion of the data waveform results in erroneous recognition of data at the receiving end.

Signals transmit along the interconnect and have a fixed propagation delay. The propagation delay is based on the medium of propagation. On a PCB it is generally FR4. The velocity of the signal on the outer layers of the PCB is 18.14 cm/nSec and internal layers is 14.09 cm/nSec. As can be seen there is a difference in propagation velocity within the PCB build. This is important to note when we have to match the timing of signals in technologies like DDRx. Propagation delay is proportional to $\sqrt{\varepsilon_r}$.

Objective of signal integrity is to analyse the behaviour of the interconnect path and to check whether the distortion in the signals are above/below the threshold levels $\mathbf{V_{IH}}$ and $\mathbf{V_{IL}}$. The driver signal has a higher value for $\mathbf{V_{IHOUT}}$ and a lower value for $\mathbf{V_{ILOUT}}$ than the receiver whose thresholds are $\mathbf{V_{IHIN}}$ and $\mathbf{V_{ILIN}}$. This difference ($\mathbf{V_{IHOUT}}$-$\mathbf{V_{IHIN}}$) is termed "Noise Margin High" and ($\mathbf{V_{ILOUT}}$-$\mathbf{V_{ILIN}}$) is called "Noise Margin Low". These values are termed "Noise Margin". Since these are voltage dependent, this would vary from logic family to logic family. When the operating voltage is lower, these noise margins are lower.

The signal path consists of the forward path and the return path. Return path is as important as the forward path and should have minimal discontinuities. There are SIX key signal integrity issues. These are detailed below.

Signal Reflection

The fact that signal path is a transmission line and signals get distorted due to the frequency dependant nature of the interconnect. The distortion is due to instantaneous impedance change in the electrical path of the signal. Common impedance discontinuities are VIA, Stub, change of signal path to different layers, connector points etc. This impedance change results in a reflection of the signal which overrides on the signal thereby distorting it. The amplitude of reflection is dependent on the change in impedance the signal sees. The reflection coefficient is defined by the equation:

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

Where $\mathbf{Z_2}$ is the instantaneous impedance the signal sees and $\mathbf{Z_1}$ is the impedance of the path from where the signal is travelling. This is the first signal integrity issue referred to as "**Reflection**".

Crosstalk Between Signals

The next aspect of signal distortion termed "**Crosstalk**" is caused by the proximity of signal paths. This is a very common interference in PCB's and packages where a number of signal lines run parallel to each other. This results in coupling between the parallel traces and contributes by the mutual inductance and mutual capacitance between

the signal path. When one of the signal paths has a signal that is switching, it induces a distortion in signal that is “quiet” (not switching). This noise generally impacts the GROUND and POWER rails, thus impacting the noise margins.

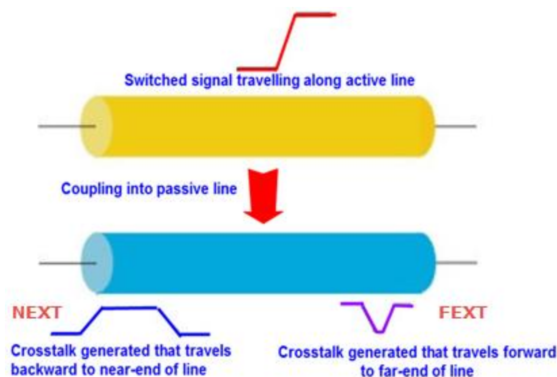

Fig 4. Crosstalk Coupling – NEXT/FEXT

As can be seen from Fig 4, there are two types of crosstalk one that occurs at the driver end, called “Near End Crosstalk – NEXT” and the other one at the receiver end called “Far End Crosstalk – FEXT”. The NEXT amplitude is governed by the inductive coupling and thus is present for the entire signal traverse time – which is twice the propagation delay from driver to receive. FEXT is at the receiver end and is dependent on the rise time of the device.

Electromagnetic Interference

The third signal integrity issue is EMI. This is due to the presence of higher harmonics in the signal. When we take the Fourier transform of the signals that are distorted (BLUE waveform) - Fig 5, it can be seen that amplitudes of higher harmonics are more than values as defined by the Fourier Theorem without distortion (RED waveform).

The loop area formed by the signal forward path and the return path behaves as a loop antenna. Higher harmonics in this results in radiation. Any discontinuity in the signal return path due to splits in power planes, slots in planes would results in higher radiation levels. EMI is due to both radiation and conduction. Conductive radiation interferes with other systems through cables and power lines. Conductive radiation can be addressed by using EMI filters at both ends.

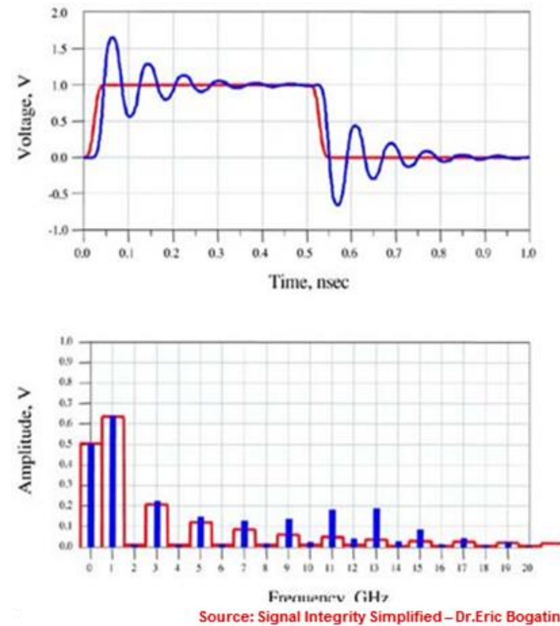

Fig 5. Harmonic Content of Signal

Radiated EMI is primarily caused by signal distortions and the signal loop area. Electromagnetic Compliance (EMC) can be achieved by proper design of interconnect geometries, PCB/packages.

Ground Bounce (SSO / SSN)

This is the fourth signal integrity issue. This is another form of Crosstalk as it impacts the ground and power rails. This is also commonly referred as SSN (**S**imultaneous **S**witching **N**oise) or SSO (**S**imultaneous **S**witching **O**utput) noise.

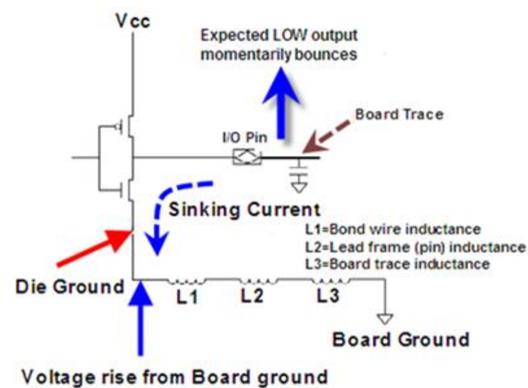

Fig 6. Ground Bounce (SSO or SSN)

This is due to the parasitics of the package used for the device. This signal distortion is

primarily associated with BUS signals. When multiple data lines use the same ground and power rail path, the sinking current is high. The voltage at the die ground and PCB ground point are not the same. Note from Fig 6, that inductances L1, L2 and L3 contribute to this voltage differential. Same is applicable for the power rail end also. The number of simultaneously switched signals decide the amplitude of this distortion. This erodes into the NMH and NML levels.

GHz signalling and Losses

Demand for higher operating speed is never ending. Signal bus widths have moved from 8 bit to over 64 bits. Parallel architecture has given way to serial data transfer technologies. This enables simpler PCB level design due to reduction of the number of signal paths. Elimination of parallel buses reduces the crosstalk.

Serial signal transmission is generally above a data rate of 1 gigabits/sec. These data rates add new aspects of signal losses / distortion. New requirements in signal handling and material aspects are now necessary.

Signal losses were primarily due to resistive effect of interconnect. At gigabit data rates, skin effect in conductors reduces conductor area available for signal propagation. This increases the resistive loss. Dielectric loss is the other contributor that becomes relevant. Dielectric loss is governed by the dielectric properties of the material.

At gigabit data rates higher frequency component of the signals are attenuated more resulting in signal rise time degradation.

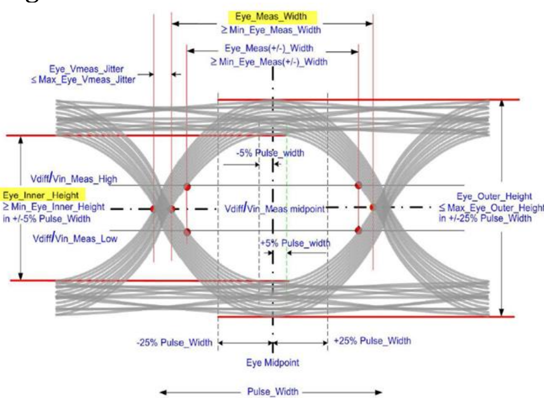

Fig 7. EYE Diagram for Gigabit Signalling

Quality of a signal transmission is measured using EYE diagram and is defined by the EYE height and width. Every gigabit signalling standard like PCIe, USB, HDMI, SATA etc. define minimum EYE width and EYE height values at both transmitter and receiver ends. From Fig 7, it can be seen that EYE height is impacted by the signal distortions and EYE width by signal propagation time of each sequential bit.

Signal losses impact rise time of the data bits. One of the key requirement for gigabit signalling is to optimise signal losses. This is the fifth signal integrity issue.

Power Delivery Network

The impact of process enhancements in semiconductor technology combined with increased device densities has resulted in reduction in operating voltages to optimize power dissipation. These designs are invariably multi-layer PCB builds using multiple power and ground planes for power delivery. Goal of a power delivery network is to provide clean power and reference voltage to the active devices on the die.

Current day device technology uses high pin count surface mount technology devices resulting in a large number of VIA's for signals and connectivity to power and ground planes. These VIA's increases the inductance of the power delivery planes. The equivalent circuit of a PDN from the point of injection at PCB level to the silicon die level is shown in Fig 8.

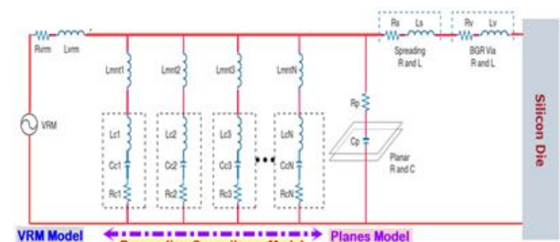

Fig 8. Power Delivery Network

PDN is thus a frequency dependant network. Effectiveness of the bulk capacitors at the voltage regulator would be up to 1MHz. Decoupling capacitors address up to 100MHz. The power plane structure extends

this to 150MHz. Beyond this the on chip capacitors provide the required bandwidth. Designing the power plane builds to balance the inductive effects of the planes by providing optimal inter-plane capacitance is one of the critical aspects of PCB stack design. A typical comparison of PCB stack build is shown in Fig 9.

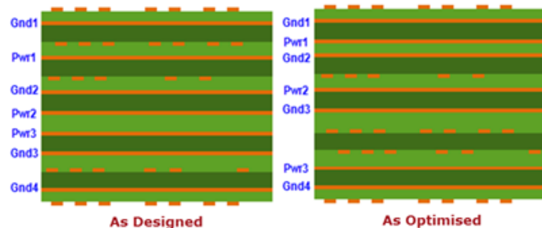

Fig 9. PCB Stack Design – Optimal Build

While designing the PDN, it is important to make appropriate choice of decoupling capacitors based on their frequency characteristics. Another deciding factor is the mounting inductance of the decoupling capacitors contributed by the via structures that connect to power planes and return path. We need to analyse the PCB level PDN behaviour up to a frequency of 100MHz. It is critical to minimise the PDN inductance. This can be achieved by proper choice of capacitor package types and fan-out structure. Fig 10 shows typical inductance values of various capacitor package types.

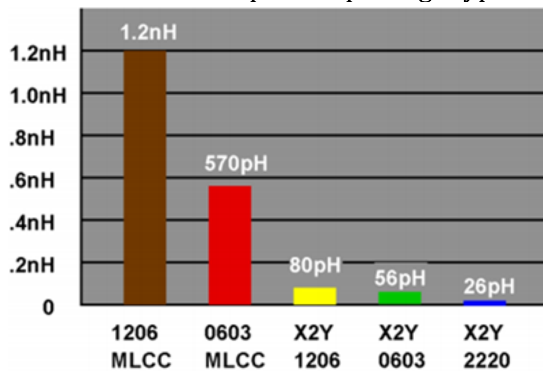

Fig 10. Capacitor Package Inductance.

To ensure a good PDN design, DC drop analysis and AC analysis are performed using Power Integrity tools like MentoGraphics Hyperlynx. DC drop analysis show cases high current densities and also depicts voltage profile of the plane.

Acceptable ripple on any voltage rail is ±5%. The PDN impedance is governed by the transient current drawn. The PDN has to meet the target impedance as defined by:

$$Z_{TARGET} = \left[\frac{VoltageRail \bullet \left(\frac{\%Ripple}{100} \right)}{MaxTransientCurrent} \right]$$

DC Drop analysis show cases critical areas of the power plane splits which normally would go unnoticed. Fig 11 shows the voltage and current density profiles of a typical PDN (Analysed using MentorGraphics Hyperlynx software.)

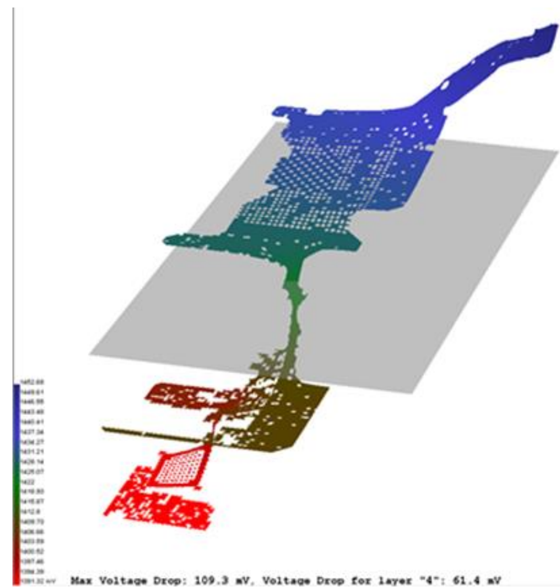

Fig 11. PDN Voltage Profile

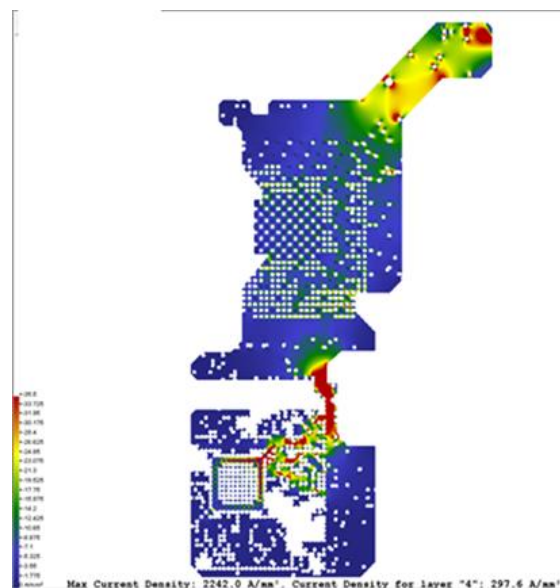

Fig 12. PDN Current Density profile.

Using simulation to identify potential power integrity problems such as DC voltage drop and excessive current density is essential for today's high-speed digital designs.

Addressing SI Issues

As seen from the above, key SI issues to be addressed are reflection, crosstalk, conductor loss and ground bounce. Since EMI is primarily due to signal distortions, addressing them at the early stages of design ensures good electromagnetic compatibility while ensuring EMI compliance to industry standards like FCC, CISPR.

Reflection is primarily due to impedance mismatches. One of the underlying principle is to go for controlled impedance designs by proper choice of PCB stack design and conductor width. Further, termination schemes, like series termination addresses most of the concerns of reflection induced distortion.

Crosstalk can be minimised by increasing the separation of the routed interconnections, reducing the length of parallelism, or using differential signalling.

Differential signalling, predominantly used for clocks, strobes in memory designs and in serial interfaces reduces the impact of distortion to a large extent.

EMI aspects are addressed by minimising the return loop area for signal traces or by providing "VIA" stitching to ground near to signal layer transitions.

Conclusion

A brief introduction to signal and power integrity issues in interconnect design is presented. This domain is vast and primary objective of this paper is to act as a curtain raiser for system designers.

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